CLAIMS

What is claimed is:

1. A self-testing random access memory system, comprising:

a memory array; and

a self-testing RAM interface embedded on a circuit board with the memory array, the self-testing RAM interface tests integrity of data stored in the memory array.

2. The system of claim 1, the self-testing RAM interface interacts with a central processing unit (CPU) to test the CPU to memory interface.

3. The system of claim 1, the self-testing RAM interface cooperates with a CPU to facilitate testing memory array data cells.

4. The system of claim 1, the self-testing RAM interface can correct errors in data stored in the memory array.

5. The system of claim 4, the self-testing RAM interface corrects errors by replacing erroneous data with redundant data stored in the memory array.

6. The system of claim 1, the self-testing RAM interface includes a microprocessor.

7. The system of claim 6, the self-testing RAM interface includes a memory component that facilitates execution of testing and/or correcting algorithms.

8. The system of claim 1, the self-testing RAM interface is implemented with discrete logic.

9. The system of claim 1, the self-testing RAM interface is implemented using SoC (System on Chip) technology.

10. The system of claim 1, the memory array is associated with a field programmable gate array.

11. The system of claim 1, the self-testing RAM interface is constructed with higher performance memory devices than the memory array including Gallium Arsenide based devices

12. The system of claim 1, the self-testing RAM interface comprises large geometry devices and ECC, wherein the large geometry and ECC make the RAM interface less susceptible to errors than the memory array.

13. The system of claim 1, the self-testing RAM interface supports multiport memory access.

14. A self-testing and self-validating memory system comprising:

one or more memory storage banks; and

at least one central processing unit (CPU) with a self-testing RAM interface subsystem for ensuring correct data retrieval.

15. The system of claim 14, the storage banks comprising standard RAM components with internal flaws.

16. The system of claim 14, the self-testing RAM interface is constructed with higher performance memory devices than the memory array including Gallium Arsenide based devices

17. The system of claim 14, the self-testing RAM interface comprises large geometry devices and ECC, wherein the large geometry and ECC make the RAM interface less susceptible to errors than the memory storage banks.

18. The system of claim 14, the self-testing RAM interface acts as a virtual memory manager and maps received data to multiple copies of the data in different memory banks to enable correct data retrieval.

19. The system of claim 18, error correction codes (ECCs) and voting mechanisms determine the most probable data value to return from amongst the multiple copies.

20. A self-correcting and self-validating device comprising:

a plurality of internal memory stores; and

a self-testing interface that maps input addresses and data to a multitude of memory cells on a plurality of memory stores to facilitate accurate data storage and retrieval, wherein the memory cells store copies of the input data.

21. The device of claim 20, error correction codes (ECCs) and voting mechanisms determine the most probable data value to return from amongst the plurality of stored copies.

22. A method of self-testing comprising:

writing values to one or more memory cells in a memory device;

reading the values stored by the one or more memory cells;

comparing the values written with the values read; and

notifying a central processing unit if any of the values written differ from the values read, wherein writing values, reading a value, comparing values, and notifying a central processing unit are performed by a self-testing RAM interface.

23. The method of claim 22, the values written correspond to a test pattern.

24. The method of claim 22, the central processing unit is notified by generating an interrupt.

25. The method of claim 22, the self-testing RAM interface is embedded on the same device as the memory cells.

26. The method of claim 22, further comprising bringing the memory device on-line for use upon successful test completion.

27. An article of manufacturing comprising a computer usable medium having computer readable stored instructions thereon to perform the method of claim 26.

28. A method for testing a central processing unit (CPU) to memory interface comprising:

loading a data pattern into CPU registers;

writing the pattern from the registers to at least a portion of memory in a memory device;

reading the data written to each memory cell;

comparing the data written with the data expected in accordance with the pattern; and

notifying the CPU if any data read is different than the data expected, wherein reading the data, comparing the data, and notifying the CPU are performed by a self-testing RAM interface.

29. An article of manufacturing comprising a computer usable medium having computer readable instructions stored thereon to perform the method of claim 28.

30. A method for detecting hard errors comprising:

writing a test pattern to a plurality of memory cells in a memory device;

reading the value of each memory cell containing a portion of the test pattern;

comparing the value read with the value written to each cell; and

recording the number times the value written did not correspond to the value read for each cell, wherein writing a test pattern, reading the value, comparing the value, and recording the number of times the value written did not correspond to the value read are performed by a self-testing RAM interface.

31. The method of claim 30, further comprising:

determining whether any cell or cells have produced erroneous results more than a threshold number of times;

determining whether any extra memory cells are available; and

mapping any cells that have produced erroneous results more than a threshold number of times to available extra memory cells.

32. The method of claim 31, further comprising notifying an exception handler if there are no available extra cells.

33. The method of claim 30, wherein data regarding the number of times a cell value did not correspond to the value read is stored in a memory component located within the self-testing RAM interface.

34. A method of reading data from a self-testing RAM device comprising:

choosing a memory address;

retrieving data from a memory location associated with the address;

determining whether the data is correct;

correcting the data if it is incorrect; and

outputting the data to the requesting device, wherein the method disclosed hereby is performed by a self-testing RAM interface.

35. The method of claim 34, wherein the self-testing RAM interface determines whether data is correct by utilizing an error correction code.

36. The method of claim 35 wherein the self-testing RAM interface corrects incorrect data by retrieving a copy of the data from another data source.

37. The method of claim 36, wherein the data source is a magnetic disk drive.

38. The method of claim 36, wherein the data source is cache memory.

39. The method of claim 36, wherein the data source is one or more standard RAM devices.

40. The method of claim 39, wherein the RAM devices contain internal flaws such that the device is not fit for ordinary use.

41. The method of claim 34, wherein the self-testing RAM interface determines whether data is correct by retrieving a copy of the data from another storage device and comparing the retrieved data and the copy.

42. An article of manufacturing comprising a computer usable medium having computer readable program code means thereon to perform the method of claim 34.